Publication Number: JP05-226052A
Date of publication of application: September 03,1993
Application Number: JP04-025428
Date of filing: February 12,1992
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[Title Of The Invention]
FORMATION OF INPUT/OUTPUT PIN FOR CERAMIC MULTI-LAYER WIRING BOARD

[Abstract]
PURPOSE: To obtain continuity of a throughhole and an input/output pin securely without forming a pad for absorbing fluctuation of positions of the throughholes.
CONSTITUTION: A substrate 1 comprising ceramic and having throughholes 2 is baked, and positions of the throughholes 2 relative to a desired reference point is measured as coordinates data. A polyimide film 3 is then formed on a surface of the substrate 1, and desired parts including the measured points in the coordinates data are etched to form via holes 4. Even where the positions of the throughholes 2 have fluctuation, therefore, input/output pins 6 and the throughholes 2 are continued to each other securely because of the via holes 4 formed on the throughholes 2.

[Claim(s)]
[Claim 1]After calcinating a ceramic substrate by which a through hole was provided in the surface, form a polyimide film in the surface of said ceramic substrate, and it ranks second to it, In a formation method of an output pin of a ceramic multilayer interconnection board which forms a viahole in a predetermined part of said polyimide film, and solders an output pin via a pad for soldering to said viahole, A formation method of an output pin of a ceramic multilayer interconnection board which measures a position of said through hole to arbitrary reference points as coordinate data beforehand before formation of said polyimide film, and is characterized by forming said viahole on said measured coordinate data after formation of said polyimide film.
[Claim 2]After calcinating a ceramic substrate by which a through hole was provided in the surface, form a polyimide film in the surface of said ceramic substrate, and it ranks second to it, In a formation method of an output pin of a ceramic multilayer interconnection board which forms a viahole in a predetermined part of said polyimide film, and solders an output pin via a pad for soldering to said viahole, Before formation of said polyimide film, a position of said through hole to arbitrary reference points is beforehand measured as coordinate data, After forming a photoresist film in the surface of said polyimide film after formation of a polyimide film, A photoresist film on said measured coordinate data among said photoresist films, After exposing, developing negatives and removing using a direct writing device, inside of said polyimide film, A formation method of an output pin of a ceramic multilayer interconnection board which removes a part where said photoresist film was removed, forms a viahole, and is characterized by removing a photoresist film which remained without being removed at the time of said development after formation of a viahole.

[Detailed Description of the Invention]
[0001]

[Industrial Application]This invention relates to the formation method of the output pin of the ceramic multilayer interconnection board used as the base of a high-density multi chip package used for a very large scale computer etc.

[0002]

[Description of the Prior Art]Conventionally, what is shown in drawing 3 is known as a ceramic multilayer interconnection board in which the output pin was formed. Drawing 3 is a sectional view of a ceramic multilayer interconnection board.

Hereafter, with reference to drawing 3, the formation method of the output pin of the conventional ceramic multilayer interconnection board is explained.

[0003]First, the substrate 51 with which the through hole 52 was formed in the surface and which consists of ceramics is calcinated, and the pad 57 is further formed on the through hole 52. The pad 57 is patterned using a photolithography and formed by depositing plating only in a pad formation schedule part selectively by an electrolytic plating method.

[0004]Subsequently, a polyimide varnish is applied to the surface of the substrate 51 in which the pad 57 was formed, and the polyimide film 53 which has a viahole to said predetermined part with photolithography method is formed using the photo mask in which only a predetermined part penetrates light. This polyimide film 53 serves as a ground at the time of soldering the output pin 56.

[0005]The pad 55 for soldering is formed in the viahole formation part of the polyimide film 53 by sputtering after formation of the polyimide film 53, and the output pin 56 is soldered on the pad 55 for soldering.

[0006]

[Problem(s) to be Solved by the Invention]However, in the formation method of the conventional output pin mentioned above, with dispersion in contraction of the substrate at the time of calcinating a substrate, while the position of a through hole shifts to an early position, dispersion produces every substrate. When a viahole is not necessarily formed always on a through hole and a viahole is not formed on a through hole at the time of formation of a viahole to a predetermined part, an output pin will stop for this reason, flowing with a through hole. It is formed in order for a pad to absorb dispersion in the position of this through hole and to make it flow through a through hole and an output pin certainly, but there was a problem that a manufacturing process became very complicated, by forming a pad.

[0007]Even if the purpose of this invention does not form the pad for absorbing dispersion in the position of a through hole, there is in providing the formation method of the output pin of the ceramic multilayer interconnection board which can make it flow through a through hole and an output pin certainly.

[0008]

[Means for Solving the Problem]In order to attain the above-mentioned purpose, after calcinating a ceramic substrate by which a through hole was provided in the surface, this invention forms a polyimide film in the surface of said ceramic substrate, and ranks second to it, In a formation method of an output pin of a ceramic multilayer interconnection board which forms a viahole in a predetermined part of said polyimide film, and solders an output pin via a pad for soldering to said viahole, Before formation of said polyimide film, a position of said through hole to arbitrary reference points is beforehand measured as coordinate data, and said viahole is formed on said measured coordinate data after formation of said polyimide film.

[0009]After calcinating a ceramic substrate by which a through hole was provided in the surface, form a polyimide film in the surface of said ceramic substrate, and it ranks second to it, In a formation method of an output pin of a ceramic multilayer interconnection board which forms a viahole in a predetermined part of said polyimide film, and solders an output pin via a pad for soldering to said viahole, Before formation of said polyimide film, a position of said through hole to arbitrary reference points is beforehand measured as coordinate data, After forming a photoresist film in the surface of said polyimide film after formation of a polyimide film, A photoresist film on said measured coordinate data among said photoresist films, After exposing, developing negatives and removing using a direct writing device, a part where said photoresist film was removed among said polyimide films is removed, a viahole may be formed and a photoresist film which remained without being removed at the time of said development may be removed after formation of a viahole.

[0010]

[Function]By measuring the position of the through hole to arbitrary reference points as coordinate data beforehand, and forming a viahole on said measured coordinate data after formation of a polyimide film before formation of a polyimide film, in this invention constituted as above-mentioned. Even if the position of a through hole varies for every substrate at the time of calcination of a ceramic substrate, a viahole is certainly formed on a through hole. As a result, it becomes unnecessary to form the pad for absorbing dispersion in the position of a through hole, and a manufacturing process is simplified.

[0011]In forming a viahole by an exposure development process, Even if it becomes unnecessary to use the mask which has the pattern defined beforehand and the position of a through hole differs in using a direct writing device for every substrate, it becomes possible to form a viahole on a through hole certainly.

[0012]

[Example]Next, the example of this invention is described with reference to drawings.

[0013]Drawing 1 is a sectional view of a substrate for describing one example of this invention.

[0014]First, as shown in drawing 1 (A), the through hole 2 is formed in the surface of the substrate 1 which consists of ceramics. This substrate 1 was calcinated after the through hole 2 was formed, and the gap has generated the position of the through hole 2 after calcination to the position before calcination with dispersion in contraction of the substrate 1 after calcination.

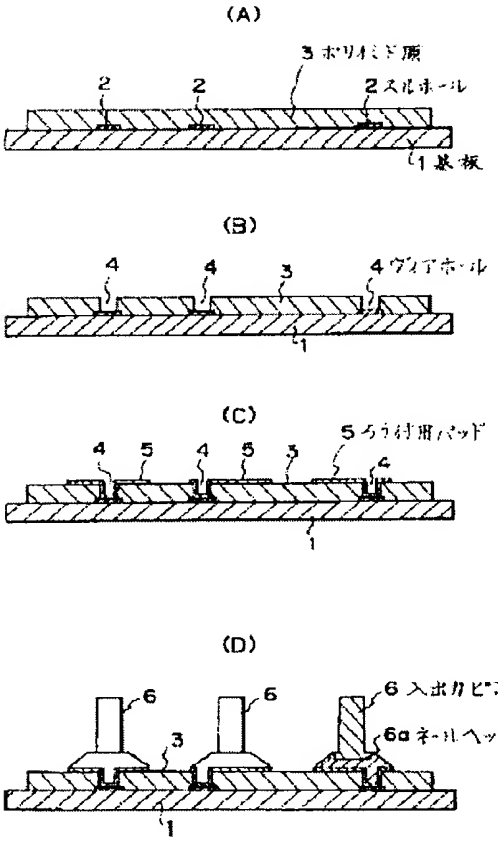
Furthermore, every substrate has dispersion.

Next, the center position of the through hole 2 is measured on the basis of arbitrary points to the substrate 1. A non-contact three-dimensional measuring instrument etc. are used for this measurement, for example, and measurement data is stored in a magnetic storage medium etc. in the form of coordinate data. After measurement of the center position of the through hole 2, apply a polyimide varnish to the surface of the substrate 1 containing the through hole 2 by predetermined thickness, it is made to harden this polyimide varnish at the temperature of about 350-400 degrees C further, and the polyimide film 3 is formed in it. As a coating method of a polyimide varnish, although which methods, such as a spin coat method, the roll coat method, or a spray coating method, may be used, a spin coat method is most generally used. When applying a polyimide varnish with a spin coat method, the rotation condition of the substrate 1 sets up suitable conditions from coating

thickness, viscosity, etc. of a polyimide varnish.
[0015]Subsequently, as shown in drawing 1 (B), the predetermined range centering on the point shown with said memorized coordinate data among the surfaces of the polyimide film 3 is etched with an excimer laser device, and the viahole 4 is formed. The power of the laser at this time is a 0.8 - 1.0 mJ/cm^2 grade, and it etches until the through hole 2 is thoroughly exposed. Thus, even if the position of the through hole 2 has shifted to the designed value or differs in etching the point on the coordinate data measured beforehand for every substrate, the viahole 4 is certainly formed on the through hole 2.
[0016]If the viahole 4 is formed, as shown in drawing 1 (C), the pad 5 for soldering will be formed in the formation part of the viahole 4, and its peripheral part among the surfaces of the polyimide film 3. The pad 5 for soldering is a plane view circle configuration.
The path is larger than the path of the nailhead 6a of the output pin 6 mentioned later.
As for the pad 5 for soldering, metal, such as Ti, Cr, or Pd, is put together, and thickness is formed in thousands - the thickness of 10,000 A of numbers.
[0017]After forming in the surface of the substrate 1 the metal thin film which consists of the above-mentioned metal by sputtering etc. as a formation method of the pad 5 for soldering, the method of masking the formation presumptive region of the pad 5 for soldering using photosensitive resist, etching the metal thin film of other parts, and using the remaining metal thin film as the pad 5 for soldering -- or, The part except the formation presumptive region of the pad 5 for soldering is masked using photosensitive resist, After forming in the surface of the substrate 1 the metal thin film which consists of the above-mentioned metal by sputtering etc., remove photosensitive resist and the metal thin film of the part except the formation presumptive region of the pad 5 for soldering is removed with photosensitive resist in that case, The method of using the remaining metal thin film as the pad 5 for soldering or the method of masking the part except the formation presumptive region of the pad 5 for soldering, and forming a metal thin film (pad 5 for soldering) only in the formation presumptive region of the pad 5 for soldering by sputtering is used.
[0018]Finally, as shown in drawing 1 (D), the nailhead 6a of the output pin 6 is soldered on the pad 5 for soldering. Since the viahole 4 is formed in the formation part of the through hole 2 at this time as mentioned above, even if it does not form the pad for absorbing dispersion in the position of the through hole 2 like before, the through hole 2 and the output pin 6 flow certainly.
[0019]Next, other examples of this invention are described with reference to drawing 2. Drawing 2 is a sectional view of a substrate for describing one example of this invention.
[0020]In this example, since the process until it forms a polyimide film on the surface of a substrate is the same as that of the example shown in drawing 1, the explanation is omitted, it swerves and it explains subsequent processes.
[0021]As shown in drawing 2 (A) after formation of the polyimide film 13, the photoresist of a positive type is applied, the surface of the polyimide film 13 is dried and the photoresist film 17 is formed in it.
[0022]Subsequently, the predetermined range centering on the point shown with the coordinate data beforehand memorized among the surfaces of the photoresist film 17 is exposed with an unillustrated direct writing device, and is developed with an alkaline developing solution. The polyimide film 13 is also etched with the photoresist film 17 by this, and as shown in drawing 2 (B), the viahole 14 is formed on the through hole 12.

[0023]It changes into the state which it exfoliates with solvents, such as n methyl 2 butanone, and shows the photoresist film 17 which remained without being removed by etching in drawing 2 (C), and the polyimide film 13 of a varnishing state is stiffened at the temperature of 350-400 degree C.
[0024]And an output pin is soldered after forming the pad for soldering like the above-mentioned example.
[0025]Like this example, when forming the viahole 14 by an exposure development process, even if the position of the through hole 12 differs in using a direct writing device for every substrate, the viahole 14 can be certainly formed on the through hole 12.
[0026]
[Effect of the Invention]By measuring the position of the through hole to arbitrary reference points as coordinate data beforehand, and forming a viahole on said measured coordinate data after formation of a polyimide film before formation of a polyimide film, in this invention, as explained above. Even if the position of a through hole varies after calcination of a ceramic substrate, a viahole is certainly formed on a through hole. Therefore, it becomes unnecessary to form the pad for absorbing dispersion in the position of a through hole, and a manufacturing process can be simplified.
[0027]In forming a viahole by an exposure development process, Since it becomes [use / a direct writing device] unnecessary to use the mask which has the pattern defined beforehand, even if the position of a through hole differs for every substrate, a viahole can be certainly formed on a through hole.
[Brief Description of the Drawings]
[Drawing 1]Are one example of the formation method of the output pin of a ceramic multilayer interconnection board of this invention a figure for explaining, and the figure (A), As for the sectional view of the substrate after polyimide film formation, and the figure (B), the sectional view of the substrate after the pad formation for soldering and the figure (D) of the sectional view of the substrate after viahole formation and the figure (C) are sectional views of the substrate after output pin soldering.
[Drawing 2]Are other examples of the formation method of the output pin of a ceramic multilayer interconnection board of this invention a figure for explaining, and the figure (A), The sectional view of the substrate after viahole formation and the figure (C) of the sectional view of the substrate after photoresist film formation and the figure (B) are sectional views of the substrate after photoresist film removal.
[Drawing 3]It is a sectional view of the conventional ceramic multilayer interconnection board.
[Description of Notations]
1 and 11 Substrate
2 and 12 Through hole
3, 13 polyimide films
4 and 14 Viahole
5 The pad for soldering
6 Output pin
6a Nailhead
17 Photoresist film

【図１】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6a ネールヘッド
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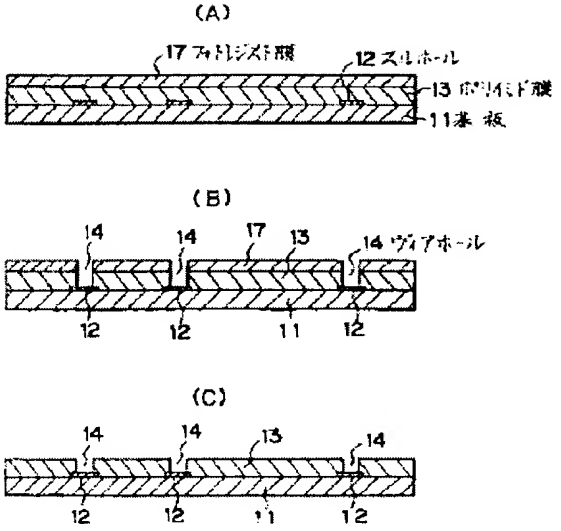
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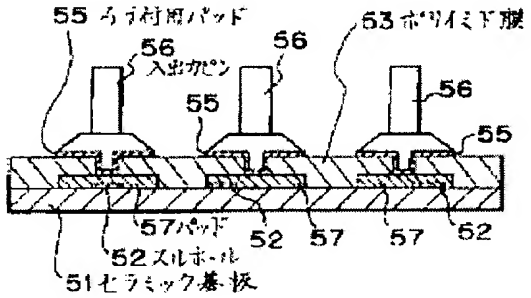
【図３】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